Thermal Analysis of AlGaN–GaN Power HFETs

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***Abstract*—In this paper, we present a thermal analysis of AlGaN–GaN power heterojunction field-effect transistors (HFETs). We report the dc, small-signal, large-signal, and noise performances of AlGaN–GaN HFETs at high temperatures. The temperature coefficients measured for GaN HFETs are lower than that of GaAs pseudomorphic high electron-mobility transistors, confirming the potential of GaN for high-temperature applications. In addition, the impact of thermal effects on the device dc, small-signal, and large-signal characteristics is quantified using a set of pulsed and continuous wave measurement setups. Finally, a thermal model of a GaN field-effect transistor is implemented to determine design rules to optimize the heat flow and overcome self-heating. Arguments from a device, circuit, and packaging perspective are presented.**

***Index Terms*—AlGaN–GaN heterojunction field-effect transistors (HFETs), high temperature, microwave, thermal effect, thermal modeling.**

I. Introduction

DUE TO GaN intrinsic properties, AlGaN–GaN heterojunction field-effect transistors (HFETs) offer important advantages for many applications in the microwave domain, including low-noise, high-power, and high-temperature applications [1], [2]. However, issues such as the reproducibility of the devices and their reliability still limit their presence in today's electronic systems [3]–[6].

Microwave transistors that can operate at high temperatures without external cooling are required for applications in the following domains:

1) aerospace;
2) automotive;
3) mineral exploration;
4) energy production [7].

The materials usually considered for providing integrated circuits (ICs) that operate in such severe environments are GaAs and Si due to their technological maturity. Optimum device designs for high-temperatures operation have already been presented for these technologies [8], [9]. However, GaN-based electronic devices has received much attention due to their inherent ability to operate at high temperatures [6], [10]. Due to its higher bandgap (3.4 eV), as compared to Si (1.1 eV) and GaAs (1.4 eV), GaN does not run into intrinsic carrier conductivity difficulties until temperatures beyond 900 K [7]. In order to provide a reliable GaN technology at high temperatures, it is necessary to evaluate the high-temperature performances of the devices from dc to microwave frequencies.

In addition, such a wide bandgap results in high breakdown fields beneficial for high-power operation; and GaN-based transistors offer important advantages for microwave power applications such as phased-array antennas and base stations. However, due to the very high power densities present in GaN-based transistors, these devices suffer from self-heating. This parasitic effect affects the devices performances [11], device reliability [12], and increases the complexity of the device model. Operating the transistors during a short period of time allows one to control the magnitude of the thermal effect [6] and, therefore, allows one to assess the impact of self-heating on the device performances. Additionally, studying devices under pulsed conditions enables one to build more robust models. Innovative measurement systems that enable one to characterize the device low-frequency, small-signal, and large-signal performance under pulsed wave (PW) have already been presented [6], [13]; they are essential to assess the impact of the thermal effects on the devices' performances.

Measurement results enable one to quantify the impact of thermal effects on an already fabricated transistor. The thermal effects result from the excess of power to dissipate [12]. This is due to the incapability of the entire system in which the device is inserted (circuit, board, package, ...) to drain enough heat away from the device active region. Since every element of the system contributes to the overall heat flow, a careful investigation must be performed to identify the critical points that must be optimized.

We present in this paper a thermal analysis of AlGaN–GaN power HFETs provided by Cree Lighting, Goleta, CA, and Cornell University, Ithaca, NY. In Section II, we present the degradation of AlGaN–GaN power HFET performances when increasing the temperature of operation up to 540 K. This study includes the impact of high temperatures on the current–voltage characteristics, high-frequency small-signal performances, microwave large-signal behavior, high-frequency noise, as well as on the matching conditions. A comparison of the measured rates with the one reported for GaAs pseudomorphic high electron-mobility transistor (pHEMT) technology is also presented. In Section III, we quantify the impact of self-heating on the current–voltage characteristics, small-signal performances, and large-signal behavior by comparing the characteristics obtained under PW and continuous wave (CW) mode of operation. Finally, in Section IV, we present a thermal model of a GaN field-effect transistor (FET). Simulations run under the CW mode in

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the presence of an RF drive allows us to determine some device design rules to minimize self-heating. Also, the means to optimize the heat flow and overcome thermal effects are presented, with arguments from a device, circuit, and packaging perspective.

II. High-Temperature Performances

In this section, we present the degradation of the current–voltage characteristics, high-frequency small-signal performances, microwave large-signal behavior, high-frequency noise, and optimum matching conditions of AlGaN–GaN HFETs when increasing the temperature of operation from 298 to 540 K.

The transfer characteristics of a transistor lead to the knowledge of the threshold voltage $(V_{\rm TH})$, saturated drain current $(I_{\rm DSS})$, and peak transconductance (peak-G_M). These parameters allow one to compare devices, they are critical to select the optimum bias point for a specific application [low noise, high gain, high output power, high power-added efficiency (PAE)], and they dominate the large-signal behavior of a transistor for operation below the cutoff frequency (f_T). When increasing the temperature of a two-finger AlGaN–GaN HFET ($L_G = 0.35\ \mu$m, $W_G = 250\ \mu$m, $I_{\rm DSS} \approx 750$ mA/mm at 300 K) up to 540 K, $I_{\rm DSS}$ changes at a rate of -3.7 mA/10 °C. It results in a reduction of the RF swing under large-signal operation, participating to the reduction of the saturated RF output power at high temperatures. Also, the peak-G_M changes with a rate of -0.25 mS/10 °C ($V_{\rm DS} = 25$ V) that results in a reduction of the cutoff frequency.

In addition to the stability circle and initial matching condition for maximum output power under large-signal operation, the small-signal characteristics lead to the determination of the cutoff frequency (f_T) and maximum frequency of oscillation $(f_{\rm MAX})$. The extrinsic f_T of the studied two-finger devices ($L_G = 0.35\ \mu$m, $W_G = 250\ \mu$m) is in the 30-GHz range at 295 K. The product $f_T \times L_G$ allows the comparison of the frequency performances with other devices regardless of the transistor dimensions. When increasing the temperature of operation up to 540 K, $f_T \times L_G$ decreases with a rate of 0.084 GHz · μm/10 °C ($V_{\rm DS} = 25$ V, $I_{\rm DS} = 70$ mA). For the studied devices, this rate results in a decrease of the cutoff frequency by 0.24 GHz/10 °C. This reduction of f_T predicted from the dc transconductance is associated to a decrease of the carrier mobility when increasing the temperature.

The high-output power capabilities of GaN-based electronic devices make them very attractive for commercial and military applications such as base stations and active phased-array radars. The power characteristics at 4 GHz of a 12-finger AlGaN–GaN HFET ($L_G = 0.35\ \mu$m, $W_G = 1.5$ mm) have been measured from 295 to 540 K at $V_{\rm DS} = 35$ V (Fig. 1). At each temperature, the load and source impedance are tuned for maximum output power at the 1-dB compression point. A relatively constant degradation of 0.138 dB/10 °C of the saturated output power is reported over the entire temperature range.

One of the primary uses of GaN-based transistors is to replace actual GaAs- and vacuum-tube-based microwave power

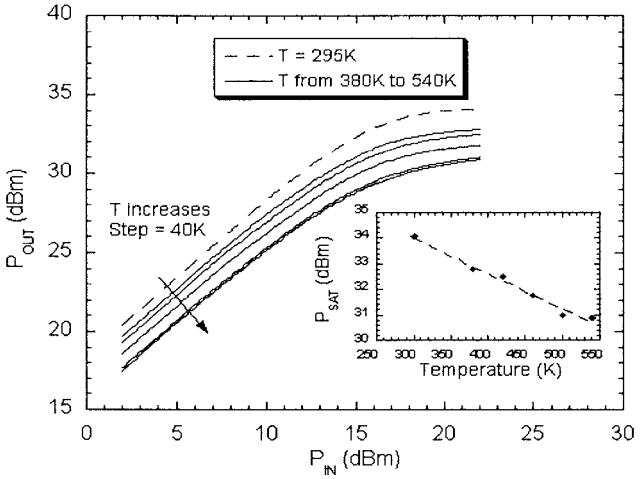

Fig. 1. Power characteristics of an AlGaN–GaN HFET ($W_G = 1.5$ mm, $L_G = 0.35\ \mu$m) at 4 GHz from 295 to 540 K.

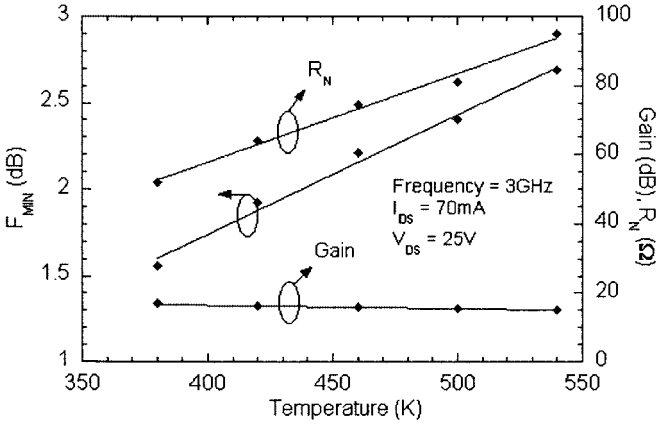

Fig. 2. Minimum noise figure, noise resistance, and associated gain at 3 GHz of an AlGaN–GaN HFET ($W_G = 250\ \mu$m, $L_G = 0.35\mu$m) from 380 to 540 K.

amplifiers (PAs) modules in high-power applications [6], [7]. However, AlGaN–GaN HFETs can also be used for low-noise amplifiers (LNA). Due to the inherent high breakdown voltage of GaN-based transistors, such low-noise devices could operate reliably without limiter devices, which would significantly decrease system noise figure and further enhance system performance. The noise parameters of two-finger AlGaN–GaN HFETs ($L_G = 0.35\ \mu$m, $W_G = 250\ \mu$m) have been measured at 3 GHz from 380 to 540 K (Fig. 2). The minimum noise figure $(F_{\rm MIN})$ and noise resistance (R_N) changes with a rate of $+0.068$ dB/10 °C, and $+2.57\ \Omega$/10 °C, respectively, while the associated gain changes by -0.114 dB/10 °C ($V_{\rm DS} = 25$ V, $I_{\rm DS} = 70$ mA). The increase of R_N when increasing the temperature of operation will result in faster degradation of the noise figure when the source impedance is moved away from the optimum termination for minimum noise figure.

The knowledge of the modification of the load and source impedance that corresponds to a specific situation (minimum noise, maximum output power, or maximum PAE) with the temperature of operation is as critical as the degradation of the device performances themselves since matching networks greatly impact circuit performances. These optimum matching conditions have been measured from 295 to 540 K during the power

TABLE I
THERMAL COEFFICIENTS OF AlGaN–GaN HFETs AND GaAs pHEMTs

	Thermal coefficient of AlGaN/GaN HFETs	Typical Thermal coefficient of GaAs pHEMTs
I_{DSS} (mA/10°C)	-3.7	
G_M (mS/10°C)	-0.25	-1.1
f_T (GHz/10°C)	-0.24	-0.5
P_{SAT} (dBm/10°C)	-0.14	-0.25
NF_{MIN} (dB/10°C)	+0.07	
R_N (Ω/10°C)	+2.6	
Ass. Gain (dB/10°C)	-0.114	

and noise measurement mentioned earlier. The measured optimum reflection coefficients are almost constant over the whole temperature range, which is beneficial to minimize the degradation of circuit performances over temperature.

Table I shows the variation with the temperature of AlGaN–GaN HFET and GaAs pHEMT characteristics. It is noteworthy that the decrease in device performances when increasing the environmental temperature is smaller for AlGaN–GaN HFETs than for devices fabricated using a GaAs pHEMT technology [8]. For instance, the f_T and $P_{\rm SAT}$ of GaAs devices have been reported to change with a rate of -0.5 GHz/10 °C and -0.24 dB/10 °C [8], [9], respectively, which is larger than the one reported in this study for GaN devices. However, it is important to mention that degradation rates vary with the device layout, structure, and process, making delicate a strict comparison between technologies. Also, it is noteworthy that the GaN devices exhibit irreversible degradation of the current–voltage characteristics after thermal cycling up to 540 K. The degradation is observed as a permanent shift of the threshold voltage and a permanent reduction of the device peak transconductance when comparing the characteristics measured before and after thermal stress. This degradation is associated with the presence of irreversible mechanisms that occur in the devices at high temperatures. If only the bandgap is considered, GaN-based electronic devices could operate up to 900 K; however, operating at high temperatures enhances all the degradation processes, and special technological processes are necessary to achieve a reliable GaN technology for high temperatures. An in-depth investigation of the metal/semiconductor contacts at high temperatures is critical to provide stability of Schottky and ohmic contacts.

III. THERMAL EFFECTS ON THE DEVICES' PERFORMANCES

In this section, we quantify the impact of self-heating on the current–voltage characteristics, small-signal performances, and large-signal behavior by comparing the characteristics obtained under PW and CW modes of operation.

A. Measurement Setups

The measurement capabilities consist of a dc/pulsed-*IV* system, a CW/PW S-parameter setup, and a CW/PW load–pull characterization bench. All the measurements in this section have been performed on-wafer and at 298 K. In the case of pulsed measurement, the current is monitored with a digitizing scope through a current probe and, when necessary, the RF power is monitored with a peak power meter. All measurements are achieved at a gate baseline that turns off the device-under-test (DUT). Both the drain and RF pulsewidth are shorter and delayed by a few 100 ns in order to be centered in the gate pulse. Fig. 3 shows a schematic of the characterization systems implemented. Details about these measurement setups can be found in [6] and [13].

B. Measurement Results

Fig. 4 illustrates the typical current–voltage characteristics of a two-finger AlGaN–GaN HFET with a total gatewidth of 250 μm and a gate length of 0.35 μm. The characteristics are measured under continuous and pulsed mode of operation. For the pulsed stimulus, the pulsewidth is 1 μs and the duty cycle is 1%; the gate baseline is chosen to turn off the device, and the drain baseline is 0 V. Under continuous mode of operation, the device exhibits a negative slope in the $I_{\rm DS}(V_{\rm DS})$ curves, which is typical of self-heating. Under pulsed mode of operation, by using the timing parameters mentioned above, the device appears to be free of thermal effects. This results in higher drain-to-source current under similar bias condition. Also, it is noteworthy from the $I_{\rm DS}(V_{GS})$ and $G_M(V_{\rm GS})$ curves, that the threshold voltage $(V_{\rm TH})$ shifts toward a lower value, and that the peak-G_M is higher and shifts toward higher $V_{\rm GS}$ values when the device is operating in a heat-free environment. The measured breakdown voltage for these devices is in the 70-V range.

Fig. 5 compares the measured f_T versus $V_{\rm GS}$ obtained under a pulsed and continuous mode of operation. The timing parameters used during the PW measurements are selected to overcome most of the self-heating effects in the device. The pulsewidth of the drain-to-source polarization was 6 μs and the duty-cycle was 6%. It is noteworthy that under pulsed operation, the cutoff frequency increases by approximately 5% compared to the CW mode. This correlates well with the dc–*IV* results showing an increase of dc transconductance when operating under pulsed mode (see Fig. 4).

Using a pulsed system to measure the RF power characteristics of a device that suffers from self-heating enables to quantify the thermal effects on the power characteristics. Fig. 6 shows the measured transducer gain of a device under a pulsed and continuous mode for different bias conditions. For this measurements, the device was tuned for maximum gain. It is noteworthy that there is a 3-dB improvement of the gain when the device operates in an isothermal environment. This result confirms the improvement in dc transconductance and cutoff frequency obtained from low-frequency and small-signal characterization.

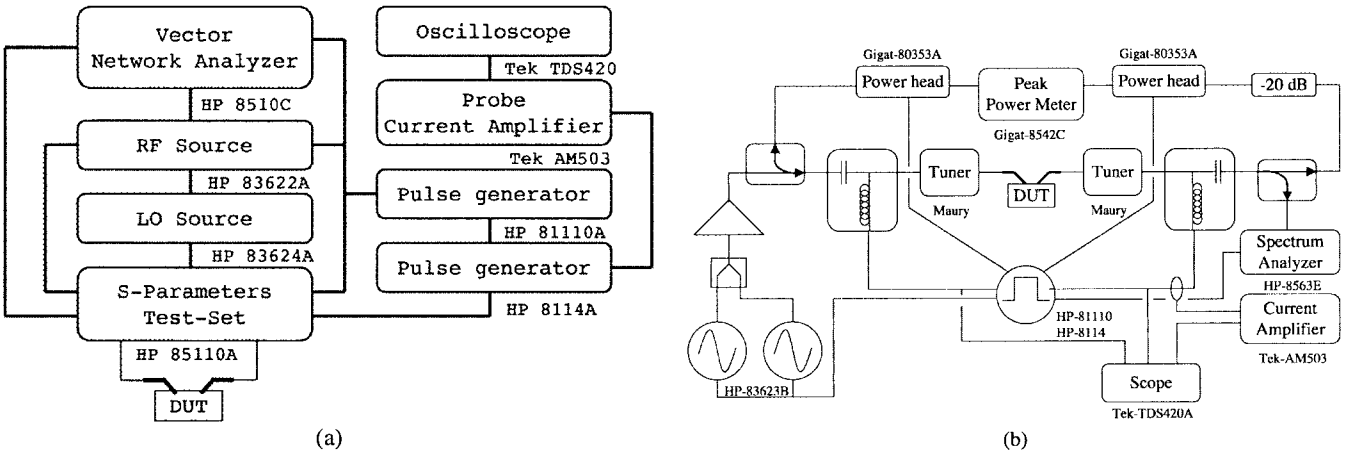

Fig. 3. Schematics of the PW/CW measurement systems. (a) S-parameter setup. (b) Load–pull setup.

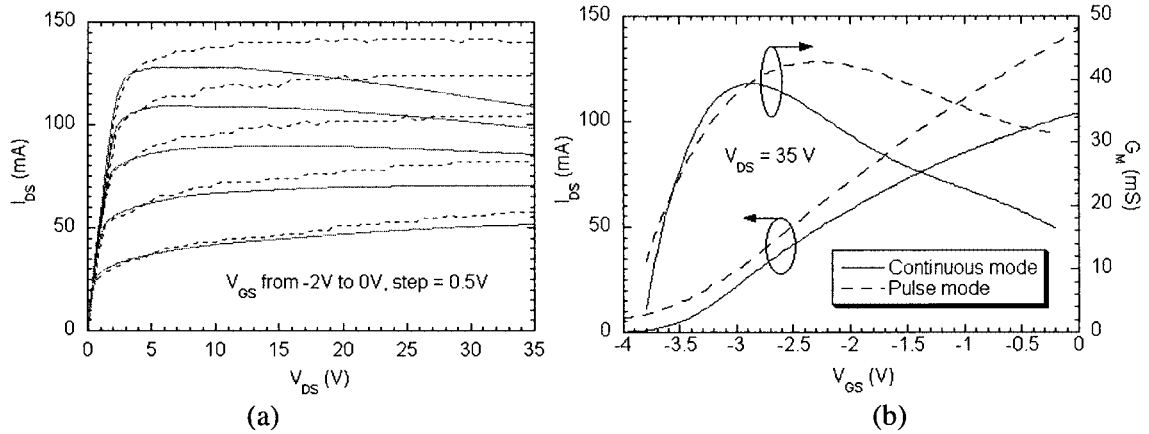

Fig. 4. (a) $I_{\rm DS}(V_{\rm DS})$ and (b) $I_{\rm DS}(V_{\rm GS})$ characteristics under continuous (solid lines) and pulsed mode (dashed lines).

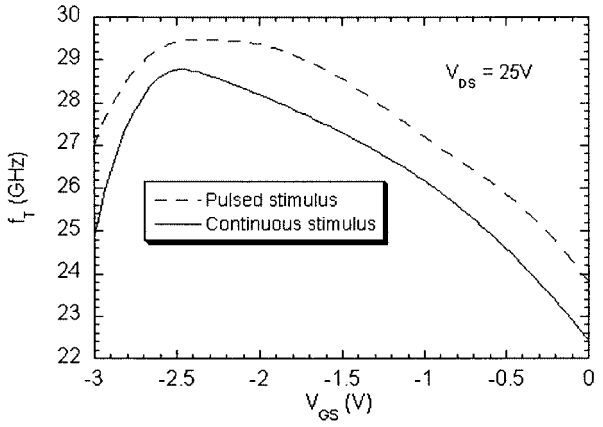

Fig. 5. Comparison of the device cutoff frequency under PW and CW operation.

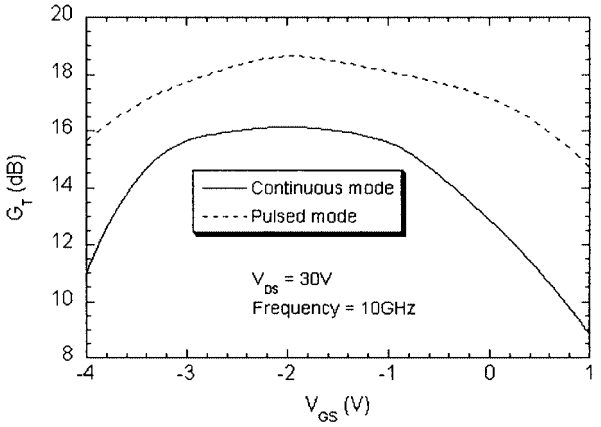

Fig. 6. Comparison of the transducer gain under CW and PW mode (base temperature $= 25\,^{\circ}$C).

IV. Temperature Analysis

A. Thermal Model

A two-finger GaN FET, with a total gatewidth of 250 μm and a gate length of 0.35 μm, grown on different substrates (SiC, Si, and sapphire) is thermally modeled by a stack consisting of an epitaxial GaN layer (thickness $= 4$ μm), a substrate (thickness $= 13$ mil), AuSn solder (thickness $= 1$ mil), and a CuMoCu base (thickness $= 80$ mil). Simulations are performed under CW operation assuming a dissipated power density of 5 W/mm of gatewidth and a base temperature fixed at 20 °C. The temperature distribution in the various layers is calculated by solving the heat diffusion equation with anisotropic temperature-dependent thermal conductivities (κ) using a finite-element method. This allows one to access the temperature distribution at any level in the device. In Section IV-C, by modi-

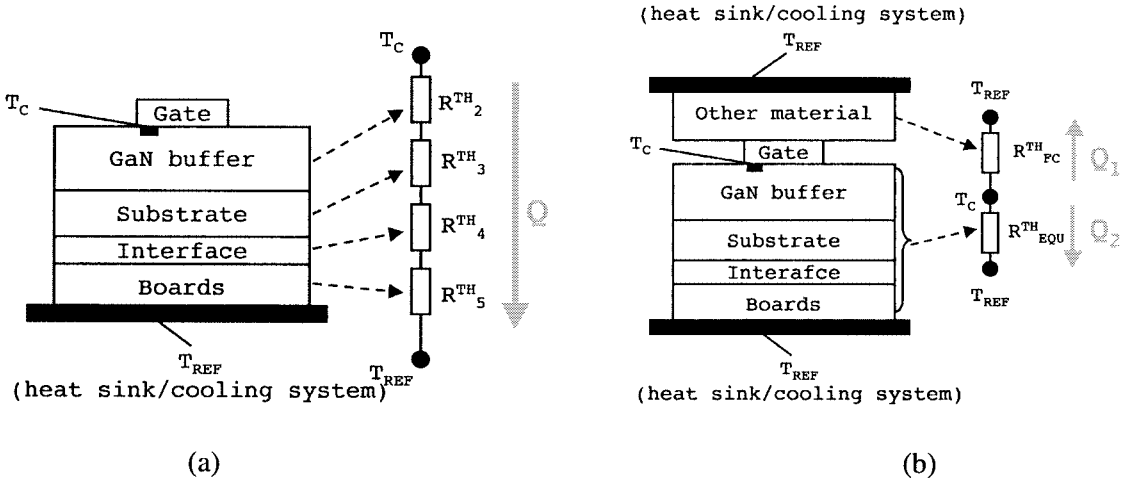

Fig. 7. Heat flow of a GaN FET in: (a) a conventional and (b) flip-chip configuration.

fying some geometrical parameters in the device model, we obtain design rules from a thermal perspective for optimum device design.

B. Heat Flow

The presence of self-heating results from the incapacity of the system in which the transistor is inserted (devices, board, interface board/device, package, and other fixtures) to drain enough heat away from the device active region. Since every element of the system contributes to the overall heat flow, a careful investigation must be performed to identify the critical points that must be optimized.

Fig. 7 shows the main elements that contribute to the heat flow in a conventional and flip-chip configuration. The heat spreads from the device channel, vertically in the different layers, and horizontally through the layers.

In a conventional configuration, the channel temperature can be approximated by

$$T_c = Q \cdot \left(\sum R_i^{\mathrm{TH}}\right) + T_{\mathrm{REF}} \tag{1}$$

and, in a flip-chip configuration, the channel temperature can be approximated by

$$T_c = Q_1 \cdot R_{\mathrm{FC}}^{\mathrm{TH}} + T_{\mathrm{REF}} = Q_2 \cdot R_{\mathrm{EQU}}^{\mathrm{TH}} + T_{\mathrm{REF}} \tag{2}$$

where R_i^{TH} is the thermal resistance associated to each layer, T_{REF} is the reference temperature fixed by the environment or a cooling system, T_{C} is the channel temperature, and Q_i represents the heat flow from the device channel to the reference temperature.

C. Design Rules

Impact of the Host Substrate: As illustrated in the results of Table II, obtained from CW simulation of a two-finger GaN FET ($W_G = 250\,\mu$m, gate−gate pitch $= 40\,\mu$m, PAE $= 50\%$) with a 5-W/mm power density to dissipate and a base temperature of 20 °C, the selection of an SiC or Si substrate instead of a sapphire substrate reduces the channel temperature by over 50%. It is noteworthy that SiC exhibits higher thermal conductivity than Si, resulting in lower device channel temperature. Also, everything being kept identical in the device structure, reducing the thickness of the host substrate results in lower thermal resistance and lower channel temperature.

TABLE II
SIMULATED CW CHANNEL TEMPERATURE FOR VARIOUS SUBSTRATES

Substrate	T_{CHANNEL} (°C)
SiC	78
Si	112
Sapphire	245

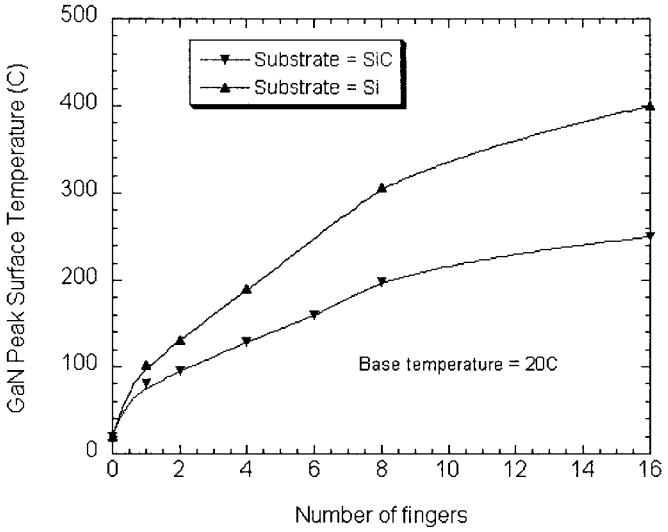

Fig. 8. GaN surface peak temperature as a function of the number of fingers.

Impact of the Number of Fingers: The number of fingers directly impacts the horizontal heat flow in the buffer layer. Fig. 8 shows the influence of the number of fingers on the channel temperature of a GaN FET grown on an SiC and Si substrate

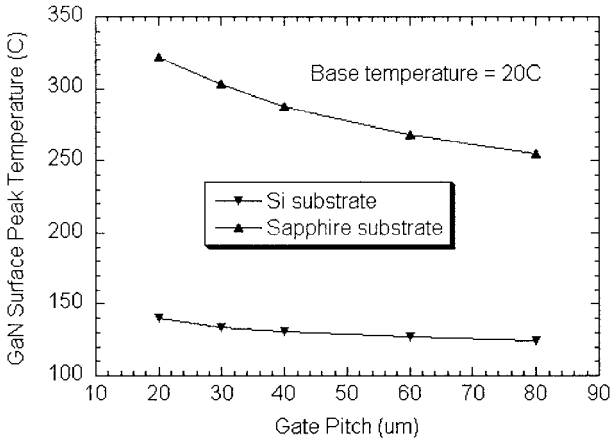

Fig. 9. GaN surface peak temperature as a function of the gate pitch for Si and SiC substrates.

in a conventional configuration. The thermal simulations are performed under a CW mode with a 5-W/mm power density to dissipate (gate–gate pitch $= 40\ \mu$m, $\mathrm{PAE} = 50\%$). Each gate finger is 125-μm long, the gate pitch is 40 μm, and the reference temperature was fixed at 20 °C. It is noteworthy that the channel temperature of the center fingers increases when increasing the number of fingers, and reaches a plateau above 14 fingers. Above 10–12 fingers, an additional finger does not lead to a significant modification of the horizontal heat flow and, therefore, does not modify the temperature of the center fingers, resulting in the observed plateau.

Impact of the Gate Pitch: The device gate pitch directly impacts the horizontal heat flow in the buffer layer. Fig. 9 shows the influence of the gate pitch on the channel temperature of a two-finger GaN FET grown on an Si and SiC substrate in a conventional configuration. The thermal simulations are performed under a CW mode with a 5 W/mm of gatewidth power density to dissipate $(\mathrm{PAE} = 50\%)$. Each gate finger is 125-μm long and the base plate is fixed at 20 °C. It is noteworthy that the channel temperature decreases by 10% when increasing the gate pitch from 20 to 80 μm.

Impact of the Device PAE: The device PAE is of significant importance for handheld applications because it has a great impact on the battery lifetime, however, its role in base stations or other high-power applications could be considered marginal since the power supply is not always a major concern for such systems. Therefore, since GaN-based devices are initially targeted for high-power applications, the device designs are often optimized for maximum output power [14]. However, by optimizing the device design for maximum PAE instead of maximum output power, magnitude of the thermal effects can be reduced [12]. Since power densities above 10 W/mm have been reported in this technology, a backoff of a few hundred milliwatts (resulting from a PAE-oriented device design) still leaves the devices with a meaningful output power level.

1) Impact of the Circuit Design: Trying to reduce the thermal effects present in a device by improving the heat dissipation through the selection of appropriate materials and device designs is a very natural approach; however, one may question the role of the circuit design on self-heating. As discussed earlier and reported in [12], the PAE plays a significant role in thermal effects since it controls the total power to dissipate in the device. When designing a PA, the input and output matching networks are implemented to optimize the transistor for a certain behavior. The performance of a PA in term of PAE can be improved by including harmonic tuning in the design of the matching networks, therefore, increasing the complexity of the circuit design results in a reduction of the thermal effects.

2) Impact of the Mounting Technique: As seen in Fig. 7, in a flip-chip configuration, the heat flow follows two parallel paths. Mounting by flip-chip a device on a very high thermal conductor like AlN results in very small overall thermal resistance and in a reduction of the channel temperature. Circuits using this technique have already been successfully demonstrated [15].

Also, using the ambient air to maintain the reference temperature results in simpler system implementation; however, due to the large power densities involved in some applications, it may be necessary to use an active cooling system to operate at reduced temperature and allow the heat to be well dissipated. As predicted by (1) and (2) and reported in [6], operating at reduced temperature overcomes self-heating in power devices.

V. Conclusion

The degradation rates with respect to the temperature of operation of key parameters, extracted from dc, small-signal, large-signal, and noise measurements have been reported for AlGaN–GaN HFETs. GaN-based transistors have exhibited lower degradation rates compared to devices fabricated using conventional semiconductors, confirming the potential of wide-bandgap semiconductors for high-temperatures applications. In addition, thermal effects on AlGaN–GaN HFETs dc, small-signal, and large-signal performances have been quantified using a set of CW and PW measurement systems. Finally, we have presented a thermal model of a GaN FET. It has allowed us to determine design rules to reduce the temperature in the devices and has led to identifying ways to improve the thermal management in power devices. Means to overcome self-heating have been discussed from a device, circuit, and packaging point-of-view.

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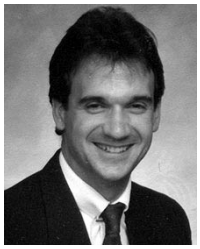

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